REMARKS

This paper is responsive to the Final Office Action mailed August 18, 2009. Claims 1-15 were pending before submission of this paper. Claims 10 and 11 are allowed, and claims 1-9 and 12-15 stand rejected. Claims 1, 7 and 12-15 have been amended, and claim 8 is been canceled. Claims 1-7 and 9-15 are currently pending. Support for all amended claims can be found in the specification, and no new matter has been added by these amendments. Reconsideration of the claims in view of the amendments and the following remarks is respectfully requested.

Claims Rejections Under 35 U.S.C. § 103

Claims 1, 4, 7, 8 and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,068,834 issued to *Ikeda* in view of U.S. Patent No. 5,982,920 issued to *Tobin*. Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Ikeda* in view of *Tobin* in view of U.S. Patent No. 7,016,526 issued to *Smilansky*. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Ikeda* in view of *Tobin* in view of U.S. Patent No. 6,408,105 issued to *Maruo*. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Ikeda* in view of *Tobin* in view of U.S. Patent No. 6,130,959 issued to *Li*. Without conceding the merits of the rejection, Applicants respectfully submit that the amended claims overcome the rejections.

The present invention relates generally to wafer inspection, and in particular to classifying defects. Specifically, claim 1, as amended, recites:

> A defect data analysis method comprising the steps of:
> obtaining defect position information by inspecting a substrate with an inspection apparatus, wherein the substrate is processed in a process of circuit pattern formation on the substrate;
> storing the obtained defect position information in memory;
> processing the defect position information stored in the memory using a processor;
> obtaining a wafer map showing a distribution shape of defects from the processed defect position information;
> classifying the obtained distribution shape of defects on the wafer map into one of a plurality of distribution shape characteristic categories by using a defect distribution shape classifier and the processed defect position information, wherein the plurality of distribution shape characteristic categories comprises: repeated defects, clustered defects,

arc-shaped regional defects, radial regional defects, line type regional defects, ring and blob type regional defects and random defects; and

displaying, on a display screen, the classified distribution shape of defects on the wafer map, wherein the distribution shape characteristic categories are each displayed using different colors.

Claim 1 describes a distribution shape of defects on a wafer map, as shown in Fig. 1. The wafer map showing the distribution shape of defects is obtained by processing defect position information obtained from a substrate. The distribution shape of defects is classified into one of a plurality of distribution shape characteristic categories by using a defect distribution shape classifier. The classified distribution of defects is then displayed on the wafer map on a display screen.

Ikeda discloses using defect position information to obtain a defect image. Only one defect image is obtained from the corresponding position information. (See col. 4, lines 33-64). However, *Ikeda* is not the same as claim 1 because *Ikeda* does not disclose that a wafer map is obtained that shows a distribution shape of defects, that the distribution shape of defects is classified based on a defect distribution shape, and that the classified distribution shape of defects is displayed on the wafer map.

Tobin fails to cure the deficiencies of *Ikeda*. The Office Action cites Fig. 7 of *Tobin* for disclosing a distribution of defects. (See Office Action, page 5). However, as shown in Fig. 7 of *Tobin*, a number of defects for each wafer is merely shown with graphs. This is not the same as a wafer map showing a distribution shape of defects as recited in claim 1.

Neither *Tobin*, *Ikeda* nor any of the other cited references, alone or in combination, teach all of the features recited in independent claim 1. Specifically, *Tobin* and *Ikeda* do not disclose "obtaining a wafer map showing a distribution shape of defects from the processed defect position information; classifying the obtained distribution shape of defects on the wafer map into one of a plurality of distribution shape characteristic categories...; and displaying, on a display screen, the classified distribution shape of defects on the wafer map." For at least this reason, claim 1 is allowable over the cited art.

Independent claims 7, 12 and 14 recite features that are similar to the features recited in claim 1. As discussed above, the cited art does not disclose these features. Thus,

claims 7, 12 and 14 are also allowable over the cited art for at least the same reasons, as well as on their own merits.

Claims 2-6 depend from claim 1, claim 9 depends from claim 7, claim 13 depends from claim 12, and claim 15 depends from claim 14. As discussed above, claims 1, 7, 12 and 14 are allowable. Thus, claims 2-6, 9, 13 and 15 are also patentable for at least the same reasons, as well as on their own merits.

Claim 8 has been canceled, rendering the rejection of this claim moot.

Accordingly, withdrawal of the rejection of claims 1-15 under 35 U.S.C. §103(a) is respectfully requested.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 206-467-9600.

Respectfully submitted,

/John J. Farrell/

John J. Farrell
Reg. No. 57,291

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 206-467-9600
Fax: 415-576-0300
JJF:kjp
62304140 v1